| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/846,410 | VON DER EMBSE, URBAIN ALFRED | |
| | Examiner | Art Unit | |
| | Jason M. Perilla | 2611 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed September 5, 2007*.

2. ☒ The allowed claim(s) is/are *claims 5-9 renumbered respectively as claims 1-5*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20071120* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## EXAMINER'S AMENDMENT

1. Claims 5-9 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Urbain A. von der Embse on November 20, 2007.

The application has been amended as follows wherein the following versions of claims 5-9 replace all prior versions in their entirety:

Claim **5**. A method for generating and applying N hybrid Walsh complex orthogonal codes for code division multiple access (CDMA), said method comprising the steps:

generating N Walsh codes W(c) with code index c=0,1,2,. . .,N-1, each with N chips where N is a power of 2,

generating said N hybrid Walsh codes $\tilde{W}(c)$ by reordering each of said N Walsh codes into a corresponding real component and a corresponding imaginary component of a hybrid Walsh code

as defined by equations

for c = 0, $\tilde{W}(c)$ = W(0) + jW(0)

for c = 1,2,...,N/2-1, $\tilde{W}(c)$ = W(2c) + jW(2c-1)

for c = N/2, $\tilde{W}(c)$ = W(N-1) + jW(N-1))

for c = N/2+1,...,N-1, $\tilde{W}(c)$ = W(2N-2c-1)+jW(2N-2c)

wherein $j=\sqrt{-1}$,

wherein said N hybrid Walsh codes are generated by reading the N Walsh codes chip values from a Walsh code memory in a digital signal processor and writing the reordered Walsh codes to a hybrid Walsh code memory,

applying said N hybrid Walsh codes in an encoder and in a decoder of a CDMA system by encoding transmitting data and decoding receiving data with ~~replacing existing said N Walsh real codes with~~ said N hybrid Walsh complex codes ~~according to a same code vector indexing~~, and

transmitting data encoded by the encoder and receiving data decoded by the decoder.

Claim **6**. A method for generating and applying spreading codes for code division multiple access (CDMA), comprising the steps:

constructing a P by P Discrete Fourier Transform (DFT) code matrix E having row vectors and column elements ~~and using said DFT matrix as a spreading code with code matrix E~~ wherein said row vectors are code vectors, ~~and~~ said column elements are code elements, and P is an integer,

constructing ~~a spreading code from~~ a hybrid Walsh code having row vectors and column elements ~~and a DFT code, said spreading code is defined by an N*P row by N*P column code matrix C~~ wherein row vectors are code vectors and column elements are code ~~chips~~ elements,

said hybrid Walsh code is defined by a N row by N column code matrix $\widetilde{W}$ where N is a power of 2,

constructing ~~said~~ a spreading code matrix C ~~is constructed~~ by a Kronecker product of said hybrid Walsh code matrix $\widetilde{W}$ with said DFT code matrix E defined by the equation

$$C = \widetilde{W} \otimes E$$

wherein the operator "⊗" is a Kronecker product operation and said spreading code is defined by an N*P row by N*P column code matrix,

applying said spreading code matrix C in an encoder and in a decoder of a CDMA system by encoding data and decoding data with ~~replacing existing real Walsh code matrix W with said hybrid Walsh complex code~~ said spreading code matrix C, and

transmitting data encoded by the encoder and receiving data decoded by the decoder.

Claim **7**. A method for implementing hybrid Walsh codes for code division multiple access (CDMA), comprising the steps:

encoding N data symbols contained in a block with respective N hybrid Walsh codes to yield N encoded data symbols for each block at the output chip rate of 1/T chips per second wherein T is the interval between chips and N is s power of 2,

wherein said encoder accepts up to N users per block ~~wherein N is s power of 2~~ and M is ~~the~~ an actual number of users represented in the block, each of said users having a data rate corresponding to one of 1,2,. . . ,N/2 data symbols per block,

wherein said encoder accepts packets from each user and writes them to memory "A" for each block, wherein a binary address index comprising a number of bits corresponding to the maximum number of users N is used for addressing said data symbols stored in memory "A" and the data symbols for each user of the block are stored in memory "A" in a hierarchy such that a particular user is selected according to a number of more significant bits of the binary address index and the data symbols of the particular user are selected according to a number of lesser significant bits of the binary address index, the number of more significant bits and lesser significant bits of the particular user being determined according to the data rate of the particular user and the total number of users M per block.

Claim **8**. Wherein said encoder ~~hybrid Walsh codes~~ in claim **5** ~~have~~ implements a fast encoding implementation algorithm, comprising the steps:

wherein said fast encoding algorithm implemented in ~~the~~ said encoder uses memory "A" for input and to support pass 1 and uses memories "B"~~,~~ and "C" to support passes 2,. . . ,M wherein N=2^M and M is an integer and uses memory "D" to store the encoded chip output from ~~the~~ a reordering pass,

writing input data symbol vector Z~~($d_0, d_1, . . ., d_{M-2}, d_{M-1}$)~~ to said memory "A" ~~wherein the~~ at binary addressing word values ~~takes address values $d_0d_1 \bullet\bullet\bullet\bullet d_{M-2}d_{M-1}$=0,1,2,. . .,N-1;~~ $d_0, d_1, . . ., d_{M-2}, d_{M-1}$,

~~wherein~~

on pass m=1, ~~reads~~ reading pairs of data symbols from "A" and ~~performs~~ performing a two-point hybrid Walsh transform on ~~the~~ two data symbols in each pair specified

by ~~the~~ a binary data addresses $d_{M-1}$~~=0,1~~ and ~~writes~~ writing the output to "B" at a reordered $d_{M-1}$ binary data address, ~~the same addresses re-labeled with the binary chip addresses $n_0$=0,1~~,

on pass ~~m-2~~ m=2, ~~reads~~ reading pairs of data symbols from "B" and ~~performs~~ performing a two-point hybrid Walsh transform on ~~the~~ two data symbols in each pair specified by ~~the~~ a binary data addresses $d_{M-2}$~~=0,1~~ and ~~writes~~ writing the output to "C" at a reordered $d_{M-2}$ binary data address, ~~the same addresses re-labeled with the binary chip addresses $n_1$=0,1~~,

on pass m=3, ~~continues this processing by~~ reading pairs of data symbols from "C" and performing a two-point hybrid Walsh transform on two data symbols in each pair ~~with the~~ specified by a binary address~~es~~ $d_{M-3}$~~=0,1~~ and writing the ~~2-point hybrid Walsh transform~~ output to "B" at a reordered $d_{M-3}$ binary data address, ~~the same addresses re-labeled with the binary chip addresses $n_2$=0,1~~,

continuing passes m=4,. . . ,M-1, M ~~continue this processing~~ using memories "B" and "C" and data binary addresses $d_{M-4}$ through $d_0$,

~~pass m=M completes the calculation of the fast hybrid Walsh transform by performing a two-point hybrid Walsh transform pass m=M on the two data symbols specified by the binary data addresses $d_0$=0,1 and writing the output to the other memory at the same addresses re-labeled with the binary chip addresses $n_{M-1}$=0,1,~~

~~write~~ writing the output of pass m=M ~~is the~~ in an encoded chip vector Z~~($n_{M-1}$, . . . ,$n_0$)~~ stored in bit-reversed order,

performing ~~wherein~~ a final reordering pass to ~~reorders~~ reorder the encoded chip vector Z and ~~stores the ordered~~ store the reordered ~~output~~ chip vector Z~~($n_0$, $n_1$, . . . ,$n_{M-2}$, $n_{M-1}$)~~ in memory "D", and

wherein said encoder ~~in said CDMA transmitter~~ reads said encoded chip vector Z in ~~said~~ "D" and overlays said encoded chip vector with long and short pseudo-noise (PN) codes to generate N chips ~~of said encoded chip vector~~ for transmission.

Claim **9**. Wherein said decoder ~~hybrid Walsh codes~~ in claim **5** ~~have~~ implements a fast decoding implementation algorithm, comprising the steps:

wherein said fast decoding algorithm implemented in said decoder uses memory "A" for input and to support pass 1 and uses memories "B" and "C" to support passes 2,.

. . .,M wherein N=2^M and M is an integer and uses memory "D" to store the decoded chip output from a reordering pass,

removing ~~wherein the decoder strips off said~~ pseudo-noise (PN) codes from ~~the~~ a received ~~N-chip~~ encoded chip vector and ~~writes~~ writing the resultant encoded chip vector Z~~($n_0$, $n_1$,. . .,$n_{M-2}$, $n_{M-1}$)~~ to said memory "A" ~~wherein the~~ at binary addressing word values ~~takes address values $n_0 n_1 \bullet\bullet\bullet\bullet n_{M-2} n_{M-1}$=0,1,2,. . .,N-1,~~ $n_0$, $n_1$,. . .,$n_{M-2}$, $n_{M-1}$,

wherein

on pass m=1, ~~reads~~ reading pairs of chip symbols from "A" and ~~performs~~ performing a two-point hybrid Walsh inverse transform on ~~the~~ two chip symbols in each pair specified by ~~the~~ a binary chip addresses $n_0$~~=0,1~~ and ~~writes~~ writing the output to "B" at a reordered $n_0$ binary data address ~~the same addresses re-labeled with the binary data addresses $d_{M-1}$=0,1,~~

on pass ~~m-2~~ m=2, ~~reads~~ reading pairs of chip symbols from "B" and ~~performs~~ performing a two-point hybrid Walsh inverse transform on ~~the~~ two chip symbols in each pair specified by ~~the~~ a binary chip addresses $n_1$~~=0,1~~ and ~~writes~~ writing the output to "C" at a reordered $n_1$ binary data address ~~the same addresses re-labeled with the binary data addresses $d_{M-2}$=0,1~~,

on pass m=3 ~~continues this processing by~~ reading pairs of chip symbols from "C" and performing a two-point hybrid Walsh inverse transform on two chip symbols in each pair ~~with the~~ specified by a binary address~~es~~ $n_2$~~=0,1~~ and writing the ~~2-point hybrid Walsh inverse transform~~ output to "B" at a reordered $n_2$ binary data address ~~the same addresses re-labeled with the binary chip addresses $d_{M-3}$=0,1~~,

continuing passes m=4, . . . ,M-1, M ~~continue this processing~~ using memories "B" and "C" and data binary addresses $n_3$ through $n_M$,

~~pass m=M completes the calculation of the fast hybrid Walsh inverse transform by performing a two-point hybrid Walsh inverse transform on the two data symbols specified by the binary chip addresses $n_{M-1}$=0,1 and writing the output to the other memory at the same addresses re-labeled with the binary chip addresses $d_0$=0,1,~~

writing the ~~write~~ output of pass m=M ~~is the data~~ in a decoded data symbol vector Z~~($d_{M-1}$,. . .,$d_0$)~~ stored in bit-reversed order,

performing ~~wherein~~ a final scaling pass that scales the decoded data symbol vector Z by ~~the~~ a ~~N-chip~~ hybrid Walsh inverse transform scaling factor ~~"1/2N"~~, ~~and~~ reorders the scaled data symbol vector, and stores the reordered data symbol vector as output vector $Z\cancel{(d_0, d_1, \ldots, d_{M-2}, d_{M-1})}$ in memory "D", and

wherein said decoder ~~in said CDMA receiver~~ reads said ~~decoded data symbol~~ output vector in ~~said~~ "D" for further processing to recover information ~~from the data symbols~~.

Claims 5-9 are renumbered respectively as claims 1-5, and the claim dependency is renumbered accordingly.

### *Allowable Subject Matter*

3. Claims 5-9 renumbered respectively as claims 1-5 are allowed.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason M. Perilla
November 20, 2007

jmp
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CHIEH M. FAN
SUPERVISORY PATENT EXAMINER